What is Claimed is:

[c1] An integrated circuit comprising:

a set of bitlines;

a set of data lines;

a coupling circuit for each respective data line that couples a first respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline; and

a circuit that maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline.

[c2] The integrated circuit of claim 1, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

[c3] The integrated circuit of claim 2, wherein each said data line is coupled to only one said bitlines and each said data line is coupled to a different bitline.

[c4] The integrated circuit of claim 1, wherein said first respective bitline maintained at said desired potential is a failed bitline.

[c5] The integrated circuit of claim 1, wherein said desired potential is ground.

[c6] The integrated circuit of claim 1, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

[c7] The integrated circuit of claim 1, wherein all said data lines in said set of data lines are arranged in a serial order and further including:

means for coupling each data line, after said data that has been coupled to said second respective bitline, to corresponding respective second bitlines.

[c8] The integrated circuit of claim 1, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

[c9] A method of replacing, in an integrated circuit having a multiplicity of data lines

and a multiplicity of bitlines, a first bitline with a second bitline comprising:

providing a set of said multiplicity of said bitlines;

providing a set of said multiplicity of said data lines;

coupling each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline; and maintaining said first respective bitline at a desired potential after said data line is coupled to said second bitline.

[c10] The method of claim 9, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

[c11] The method of claim 10, wherein each said data line is coupled to only one said bitlines and each said data line is coupled to a different bitline.

[c12] The method of claim 9, wherein said first respective bitline maintained at said desired potential is a failed bitline.

[c13] The method of claim 9, wherein said desired potential is ground.

[c14] The method of claim 9, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

[c15] The method of 9 wherein all said data lines in said set of data lines are arranged in a serial order and further including:

coupling each data line, after said data that has been coupled to said second respective bitline, to corresponding respective second bitlines.

[c16] The method of claim 9, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

[c17] A content addressable memory comprising:

a set of bitlines;

a set of data lines, a number of said data lines less than a number of said bitlines;

a set of read lines, a number of said read lines equal to said number of said data lines, each said read line coupled to one corresponding bitline

of said set of bitlines;

means for coupling each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline;

means for directing a first respective read line coupled to said first respective bitline to a second respective read line coupled to said second respective bitline in response to said steering signal; and

means for maintaining said first respective bitline at a known fixed state after said data line is coupled to said second bitline.

[c18] The content addressable memory of claim 17,wherein all said data lines in said set of data lines are arranged in a serial order and all said read lines in said set of read lines are arranged in a serial order and further including:

means for coupling each data line, after said data that has been coupled to said second respective bitline, to corresponding respective second bitlines; and

means for switching each read line, after said read line that is switched to said immediately adjacent read line, to corresponding immediately adjacent read lines

[c19] The content addressable memory of claim 17, further including:

one or none bitlines between said first respective bitline and said second respective bitline; and

one or none read lines between said first respective read line and said second respective read line.

[c20] The content addressable memory of claim 17 wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines and is derived from fuse latches.